

Analog Signal Processing Circuits Using Floating Gate MOS Transistors

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Abstract – Low voltage non-linear computational circuits useful for analog VLSI signal processing applications based on floating gate MOS transistors (FGMOSFETs) are presented. The FGMOS transistors operate in the saturation region. The variable equivalent threshold voltage (V_T) of the FGMOS transistor is exploited in such a way to transform it to a simple MOSFET of zero V_T . A bias circuit using a conventional V_T extractor circuit makes the transformation. The transistor behaves as a simple squaring element in this case. A four-quadrant multiplier and a Euclidean norm calculator circuit are presented as applications. The most important advantages of the four-quadrant multiplier are rail-to-rail dynamic input range, low distortion and very good linearity. The main advantages of the Euclidean norm calculator circuit are unipolar supply voltage, linear expansion requiring only one FGMOS per additional input and very good linearity. SPICE simulation results verify the accuracy of the circuits.

Index Terms – Floating gate MOSFETs, V_T cancellation circuit, four-quadrant multiplier, Euclidean norm calculator circuit, analog VLSI signal processing.

I. INTRODUCTION

Analog VLSI in signal processing systems plays an increasingly important role [1,2]. The role of the analog part in mixed signal VLSI chips depends on the type of signal processing system it refers to. Two general categories are recognized, mixed analog/digital and mixed digital/analog systems. In mixed analog/digital chips the analog part provides the I/O interface to the core of the digital chip. Data converters, amplifiers, filters, power drivers, sensor interfaces are some of the analog circuit blocks which may be included to the interface. In mixed digital/analog systems the digital part provides the I/O part to the core of the analog chip. Low-precision massively parallel interconnected systems such as artificial neural networks and fuzzy controllers belong to the second category. Four-quadrant multipliers, programmable synaptic elements, winner-take-all circuits, analog memories are some of the analog building blocks used in this category. Cost, area-efficiency, low-power consumption, and linearity are some of the desired characteristics of analog signal processing circuits.

Analog computational circuits are designed to perform operations such as multiplication, squaring, square root, log and anti-log of variables, vector calculations and defuzzification. These circuits can manipulate single-ended and/or balanced inputs with the largest possible dynamic

input range featuring small nonlinearity error and low distortion. Four-quadrant analog multipliers are important building blocks in neural networks, fuzzy controllers, wireless communications and electronic systems such as voltage controlled oscillators and filters, modulation and demodulation circuits, adaptive filters, automatic gain control, frequency mixers etc. They can be used for waveform generation and modulation, and power measurements. Other typical applications also include the implementation of dividers and square-rooters, through feedback configuration. One of the design techniques for a CMOS analog squarer/multiplier is based on the square-law characteristics of a MOS transistor in saturation [3-9].

The FGMOS transistors have been used as nonvolatile analog memories in neural network processor design, in op-amp compensation, D/A and A/D converters, electronic programming and OTAs. The last years there is an increased number of publications on the use of FGMOS structures in the implementation of analog computational circuits, such as voltage squarers, multipliers and attenuators [10-17]. The drain current of a FGMOS in saturation is proportional to the square of the weighted sum of its input signals [10-17].

In this paper a zero-threshold FGMOS transistor operating in the saturation region, is used as the basic analog building block acting as a simple squarer. A bias voltage generator circuit creating a zero-threshold FGMOSFET is presented. A four-quadrant multiplier and a Euclidean norm calculator circuit are constructed based on the simple squarer. The advantages of the squarer/multiplier are low voltage, low power, rail-to-rail dynamic input range, and low distortion. The main advantages of the Euclidean norm calculator circuit are unipolar supply voltage, linear expansion requiring only one FGMOS per additional input, very good linearity and increased input range. Avoiding the use of an op-amp and feedback resulted in a better and simpler implementation compared to an earlier presented similar circuit [18].

The paper is organized as follows. The structure and the operation of the FGMOS transistor are described in section II. In section III, a zero-threshold FGMOS transistor operating in the saturation region is presented and its operation as a squarer is explained. In the same section the bias voltage generator circuit for V_T cancellation is presented. In section IV a four-quadrant voltage multiplier is proposed. In section V, a Euclidean norm calculator circuit is constructed based on the simple squarer. In

section VI SPICE simulation results are given verifying the theoretical analysis and demonstrating the feasibility and the effectiveness of the proposed circuits. Conclusions are drawn in section VII.

II. THE FGMOS TRANSISTOR

The basic structure of a N -channel floating-gate MOS transistor with n -input voltages V_1, V_2, \dots, V_n , is shown in Fig.1a. The floating-gate is formed by the first polysilicon layer over the channel while the n -input gates are formed by the second polysilicon layer and they are located over the floating gate. The floating gate is capacitively coupled to the n -input gates [19]. The symbolic representation of this device is shown in Fig.1b.

The drain current of a N-FGMOS transistor with n -input gates in the saturation region, neglecting the second order effects is given by the following equation [10-17] :

$$I_D = \frac{\beta}{2} \left(\sum_{i=1}^n k_i V_i - k_s V_s - V_{TN} \right)^2 \quad (1)$$

where $\beta = \mu_o C_{OX}(W/L)$ is the transconductance parameter of the transistor, μ_o the electron mobility, C_{OX} the floating-gate oxide capacitance, W/L the transistor aspect ratio, k_i , k_s are the capacitive coupling ratios, V_s is the source voltage and V_{TN} is the threshold voltage of the transistor. The input capacitive coupling ratios k_i are defined as

$$k_i = \frac{C_i}{C_T} \quad (2)$$

where C_i is the input capacitance between the floating gate and each of the i -th input (see Fig.1), C_T is the total capacitance associated with the floating gate, which in the saturation region is given by

$$C_T = 2C_{OX}/3 + C_{FS} + \sum_{i=1}^n C_i \quad (3)$$

where $(2C_{OX}/3)$ is the gate-to-source capacitance in the saturation region and C_{FS} is the overlap capacitance between floating-gate and source. It is assumed that the overlap capacitance between floating-gate and drain C_{FD} and the parasitic capacitance between floating-gate and bulk C_{FB} are very small compared to the C_T . The k_s capacitive coupling ratio associated with the overlap capacitances are given by: $k_s = [1 - (C_{FS}/C_T) - (2C_{OX}/3C_T)]$. It should be noted that the capacitances C_{OX} , C_{FS} , C_{FD} are proportional to the channel width (W) of a MOS transistor. The capacitances C_{OX} , C_{FS} are given by $C_{OX} = C_{OXO} L W$, $C_{FS} = C_{GSO} W$ where C_{OXO} is the floating-gate oxide capacitance per unit area, C_{GSO} is the gate to source overlap capacitance per unit channel width. Equation (1) shows that the FGMOS transistor drain current in saturation is proportional to the square of the weighted sum of the input signals, where the weight of each input signal is determined by the capacitive coupling ratio of the corresponding input.

Since direct DC simulation of the floating gate devices is not possible due to the floating node of the gate of the MOS transistor, the most common approach is based on a description of the device as a MOS transistor capacitively coupled with the control gates which additionally includes controlled voltage sources between the FG node and ground [20,21].

III. ZERO-THRESHOLD FGMOS TRANSISTOR

In a multiple input FGMOS transistor one of the control gates can be used to modulate its threshold voltage value. The device can be thought as a variable threshold transistor [1,19]. Taking $V_s=0$, (1) can be written as

$$I_D = \frac{\beta}{2} \left(\sum_{i=1}^n k_i V_i - V_{TN} \right)^2 = \frac{\beta}{2} \left(\sum_{i=1}^{n-1} k_i V_i + (k_B V_B - V_{TN}) \right)^2 \Rightarrow I_D = \frac{\beta}{2} \left(\sum_{i=1}^{n-1} k_i V_i - V_{TN}^* \right)^2, \quad V_{TN}^* = V_{TN} - k_B V_B \quad (4)$$

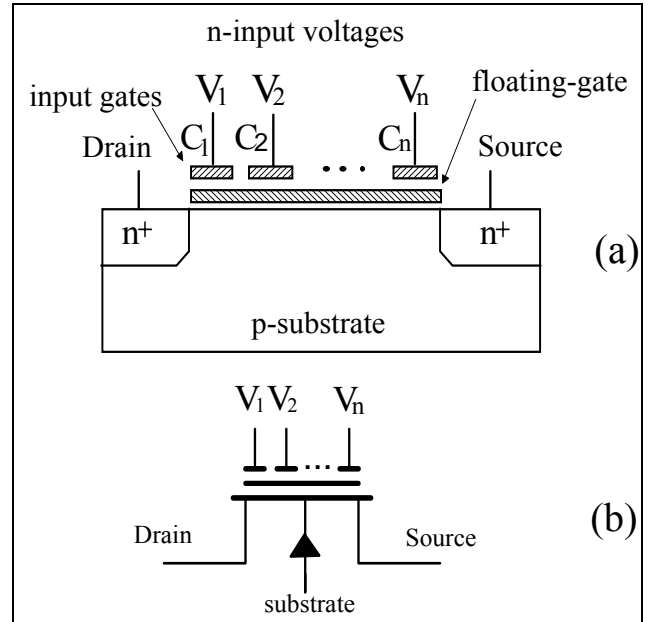


Fig. 1 Structure of a n -input floating gate MOS transistor (a) and symbolic representation (b)

Equation (4) shows the possibility of electronically tuning the threshold voltage, as seen by the other inputs of the transistor. This property has been used in neural network applications [1]. A special case of (4) is that for which

$$V_{TN}^* = 0 \Rightarrow k_B V_B = V_{TN} \quad (5)$$

For a two-input FGMOS transistor where one input is biased with voltage V_B such that (5) is valid, (4) combined with (5) leads to

$$I_D = \frac{\beta}{2} \left(k_i V_i - V_{TN}^* \right)^2 \stackrel{(4)}{=} \frac{\beta}{2} k_i^2 V_i^2 \quad (6)$$

I_{off} is given by

$$(15) \quad (V_1=V_2=0) \Rightarrow I_{off} = \frac{\beta}{2} k^2 (-2V_{SS})^2 \quad (18)$$

I_{out} is given then by

$$I_{out} = I_S + I_{off} - (I_1 + I_2) \stackrel{(15),(16),(17),(18)}{=} \beta k^2 V_1 V_2 \quad (19)$$

The output current is proportional to the product of the input voltages with a constant of proportionality which depends on the aspect ratio of the transistors.

V. A EUCLIDEAN NORM CALCULATOR CIRCUIT

The Euclidean norm of a n-dimensional vector $\mathbf{X}=(x_1, x_2, \dots, x_n)$ is defined as

$$\|\mathbf{X}\| = \sqrt{\sum_{i=1}^n x_i^2} \quad (20)$$

The Euclidean norm is necessary for calculating the unitary vector in the direction of a given vector \mathbf{X} ($\mathbf{X}/\|\mathbf{X}\|$). Therefore, it is used in calculating the angular similarity function of two vectors, for kernel orthonormalization, and to implement specific neural algorithms for image recognition/classification such as competitive learning and Adaptive Resonance Theory (ART).

A high precision CMOS Euclidean distance norm circuit was presented in [18]. Based on the zero-threshold FGMOS transistor the alternative circuit shown in Fig. 4 is presented [23].

The bias circuit generates a V_B bias given by (5), so that the FGMOS transistors M1-MN as well as MP operate in saturation for positive inputs and in such a way that (6) is valid. Then

$$\begin{aligned} I_{DP} &= \sum_{i=1}^N I_{Di} \Rightarrow \\ \frac{\beta_P}{2} (V_{DD} - V_O - V_{TP})^2 &= \frac{\beta_N}{2} k_1^2 \sum_{i=1}^N V_i^2 \\ V_O &= V_{DD} - V_{TP} - k_1 \sqrt{\frac{\beta_N}{\beta_P}} \sqrt{\sum_{i=1}^N V_i^2} \end{aligned} \quad (21)$$

Equation (21) shows that the output V_o is proportional to Euclidean norm of the input vector. For proper input voltage operation, all FGMOS transistors M_i , must operate in saturation. Then the following relation is valid for the transistor that accepts the maximum input $V_{i_{max}}$

$$\begin{aligned} V_{GD,i_{max}} &\leq V_{TN} \Rightarrow k_1 V_{i_{max}} + V_{TN} - V_O \leq V_{TN} \Rightarrow \\ V_{i_{max}} &\leq \frac{V_{DD} - V_{TP}}{k_1} - \sqrt{\frac{\beta_N}{\beta_P}} \|V_i\| \end{aligned} \quad (22)$$

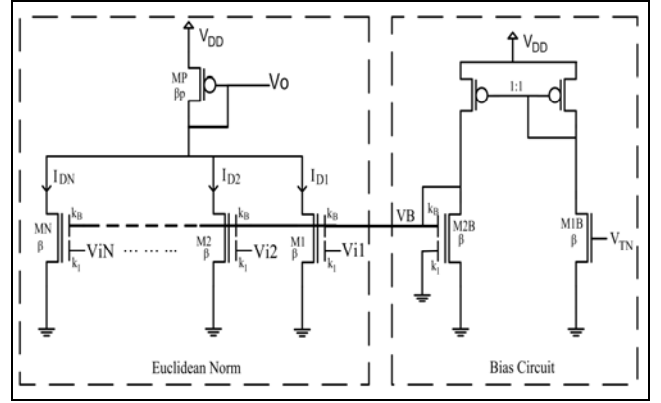


Fig. 4 A Euclidean norm calculator circuit using zero-threshold FGMOS transistor.

Equation (22) is not very functional as it relates the total vector norm with the maximum input. A more functional form for proper input voltage operation results from (22) as

$$V_{i_{max}} \leq \|V_i\| \quad (23)$$

Consequently, if V_i norm is limited as

$$\|V_i\| \leq \frac{V_{DD} - V_{TP}}{k_1} - \sqrt{\frac{\beta_N}{\beta_P}} \|V_i\| \quad (24)$$

then

$$\|V_i\| \leq \frac{V_{DD} - V_{TP}}{k_1 \left(1 + \sqrt{\frac{\beta_N}{\beta_P}}\right)} \quad (25)$$

If (25) is valid which limits the total norm, then since (24) is valid, (23) will be valid as well, ensuring proper operation.

Compared to the circuit presented in [18], this circuit is a simpler implementation of a Euclidean norm calculator, using unipolar supply voltage, having increased input range and avoiding the use of an op-amp and feedback.

VI. SPICE SIMULATION RESULTS

A. FOUR-QUADRANT MULTIPLIER

The four-quadrant multiplier and the Euclidean norm calculator circuit were simulated using SPICE in MIETEC CMOS 2.4 μm technology. A dc-macromodel [20, 21] is used. The supply voltage is $\pm 2.5\text{V}$ and rail-to-rail input range is assumed. To obtain a rail-to-rail input range and minimum nonlinearity, the capacitance coupling ratios are $k_b=0.6$, $k=0.15$. The aspect ratios of the n-MOS transistors are $(W/L)_1=(W/L)_2=(W/L)_3=(W/L)_4=10/10$ and of the p-MOS transistors $(W/L)_{p1}=(W/L)_{p2}=100/10$, $\beta_N=57 \mu\text{A}/\text{V}^2$, $\beta_p=17 \mu\text{A}/\text{V}^2$, $V_{TN}=V_{TP}=0.9\text{V}$ for MIETEC 2.4 μm technology.

Figure 5 shows the simulated dc transfer characteristics of the multiplier output current versus V_1 with V_2 as parameter. The voltage V_1 varied rail-to-rail with

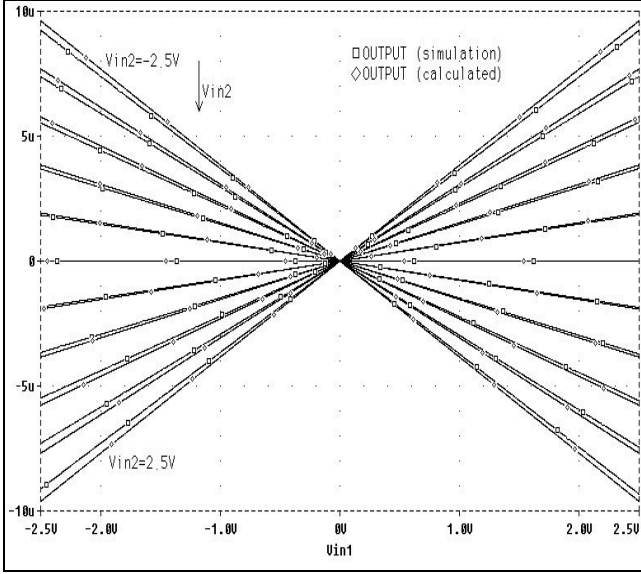


Fig. 5 DC transfer characteristics of the output current of the four-quadrant multiplier.

the voltage V_2 taking the values -2.5 to $+2.5$ V in 0.5 V increments. The worst case distortion for the voltage V_1 , was less than -40 dB. In the same figure the theoretical curves are shown as well. The circuit exhibits good linearity. Small deviations between theoretical and simulated curves are mainly due to: a) channel length modulation, b) mobility degradation.

Fig. 6 shows an output current waveform of the multiplier when two sinusoidal signals are applied. Voltage V_1 was 5 Vp-p, 1 MHz, while voltage V_2 was 5 Vp-p, 50 KHz. The spectrum of the multiplier output is shown in Fig. 7 where the two main component frequencies 950 KHz and 1050 KHz are shown. Fig. 8 shows a magnified version of Fig. 7 in the area of frequencies of interest. As can be seen, the harmonics due to nonlinearities are suppressed to at least 40 dB below the main components.

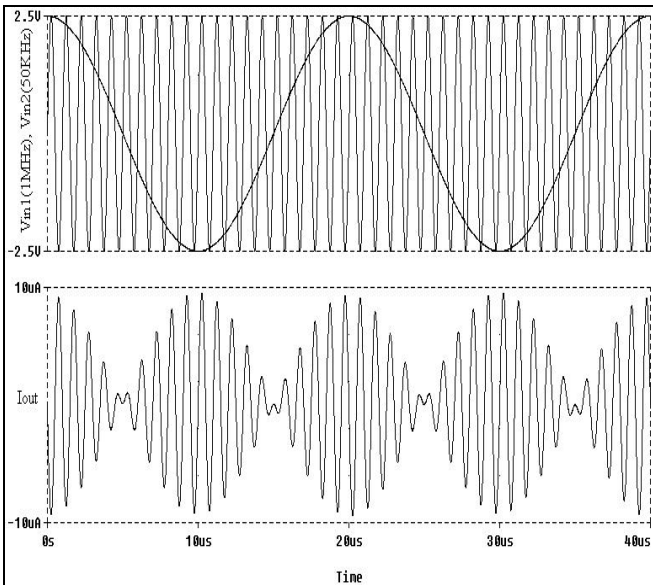


Fig. 6 Input waveforms of the four-quadrant multiplier when V_1 is a 5 V(p-p) 1 MHz sinusoidal signal, and V_2 is 5 V(p-p) 50 KHz sinusoidal signal (upper curve). The current output waveform is shown in the lower curve.

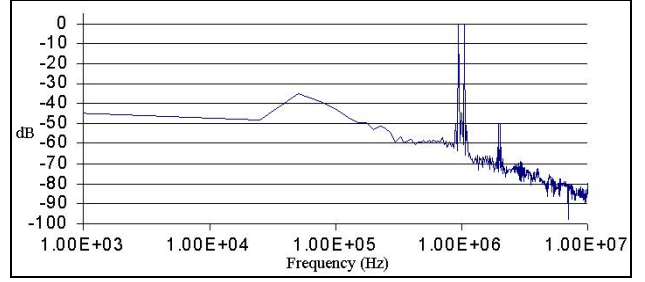


Fig. 7 Spectrum of the multiplier output when V_1 is a 5 V(p-p) 1 MHz sinusoidal signal, and V_2 is 5 V(p-p) 50 KHz sinusoidal signal.

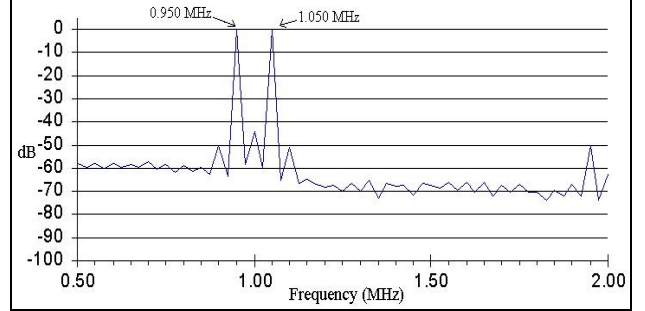


Fig. 8 Spectrum of the multiplier output when V_1 is a 5 V(p-p) 1 MHz sinusoidal signal, and V_2 is 5 V(p-p) 50 KHz sinusoidal signal focused in the frequency area of interest.

B. EUCLIDEAN NORM CALCULATOR CIRCUIT

The circuit of Fig. 4 was simulated in CMOS MIETEC $2.4 \mu\text{m}$ technology, using the two-input dc FG MOS macromodel [23], with $k_B=0.6$, $k_I=0.3$, $(W/L)_i=(W/L)_B=10/10$, whereas the aspect ratio of MP transistor is $(W/L)_P=100/10$, and $\beta_N=57 \mu\text{A}/\text{V}^2$, $\beta_P=17 \mu\text{A}/\text{V}^2$, $V_{TN}=V_{TP}=0.9$ V.

The circuit was implemented with three inputs and the transient response was checked for time-varying inputs of constant Euclidean norm. The inputs where ($f=1$ kHz)

$$V_1 = \frac{1}{k_1\sqrt{2}} \sin 2\pi f t, V_2 = \frac{1}{k_1\sqrt{2}} \cos 2\pi f t, V_3 = \frac{1}{k_1\sqrt{2}} \Rightarrow \sqrt{\sum V_i^2} = \frac{1}{k_1} \quad (26)$$

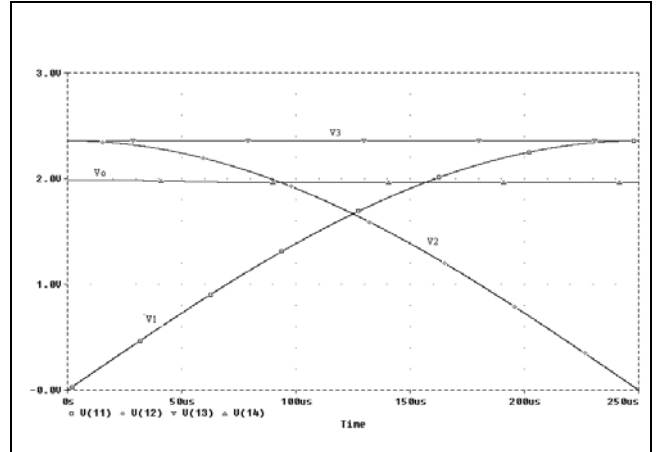


Fig. 9 The inputs and the output of the Euclidean norm calculator circuit of Fig. 4, where the inputs have a constant norm, and are given by (26).

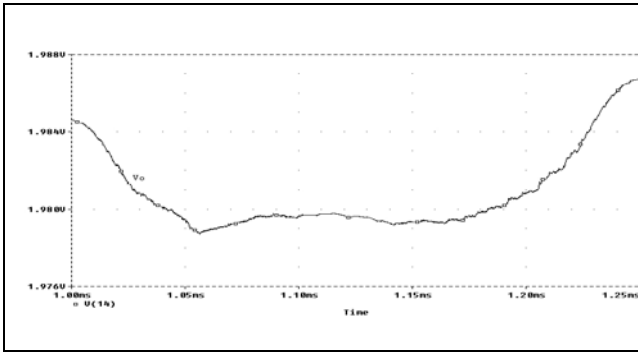


Fig. 10 Magnification of output shown in Fig. 9, where the small variations of the output about its mean value are evident.

Simulation results are shown in Fig. 9. In Fig. 10 the output is magnified, so that small variations about the mean value are obvious. After substituting the technological parameters as well as (26) in (21), and subtracting the offset term $V_{DD}-V_{TP}$, the theoretical value of the output amplitude is equal to $V_{o,theor}=590$ mV. The simulated value calculated from Fig. 9, is equal to $V_{o,sim}=615\pm 3.5$ mV, corresponding to a deviation from the theoretical value 4.2%, whereas the deviation of the output voltage about the mean value is 0.5%. The deviation of the simulated value from the theoretical one, is due to the following reasons: a) the deviation of the theoretical k_1 value from the one used in the simulations, due to the difficulty of calculating the parasitic capacitances, and b) to the channel length modulation. Channel length modulation has a stronger effect to this circuit compared to the circuit presented in [18], because the V_{DS} voltage of the squaring elements of the circuit presented here does not remain constant during operation, as opposed to [18]. The very small variation of the output about its mean value is an indication of satisfactory linearity of the FGMOS transistors as squaring elements, verifying (6).

VII. CONCLUSIONS

A zero-threshold FGMOS transistor operating in the saturation region is used as a basic building block to construct analog computational circuits. A proper bias generator circuit such as to cancel the transistor threshold voltage is presented. The transistor behaves as a simple squaring element in this case. A four-quadrant multiplier and a Euclidean norm calculator circuit are constructed based on the zero-threshold FGMOS squaring element. The Euclidean norm uses unipolar supply voltage and can be expanded linearly using one transistor per additional input. The four-quadrant multiplier and the Euclidean norm calculator circuit were simulated using SPICE and MIETEC 2.4 μ m CMOS process parameters. Spice simulation results for the four-quadrant multiplier show good agreement with theoretical predictions. Small deviations are mainly due to the channel length modulation and mobility degradation. Spice simulation results for the Euclidean norm calculator circuit show very good linearity. However, silicon implementation of the proposed circuits would require techniques for elimination of trapped charge in the floating-gate, produced by etching [24].

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